PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classificati n 6 :
G11B 5/39, 5/33, 5/035

A1

(11) International Publication Number: WO 96/18189

(43) International Publication Date: 13 June 1996 (13.06.96)

(21) International Application Number: PCT/US95/16212

(22) International Filing Date: 8 December 1995 (08.12.95)

(30) Priority Data:
08/353,681 9 December 1994 (09.12.94) US

(71) Applicant: CONNER PERIPHERALS, INC. [US/US]; 3081 Zanker Road, San Jose, CA 95134-2128 (US).

(72) Inventors: SHRINKLE, Louis, J.; 1856 Wilstone Avenue, Leucadia, CA 92024 (US). SCHWALL, Matthew; 1363 Shinly Place, Escondido, CA 92026 (US).

(74) Agent: FAIRBAIRN, David, R.; Kinney & Lange, P.A., Suite 1500, 625 Fourth Avenue South, Minneapolis, MN 55415-1659 (US).

(81) Designated States: CA, CN, JP, KR, MX, SG, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: APPARATUS FOR COMPENSATING FOR NON-LINEAR CHARACTERISTICS OF MAGNETORESISTIVE HEADS

(57) Abstract

An apparatus that compensates for the asymmetry and the baseline shift in the signal generated by a magnetoresistive head. The apparatus stores a first correction factor for the baseline shift, a second correction factor for correcting the amplitude of positive portion of the signal and a third correction factor for correcting the amplitude of negative portion of the signal. The first correction factor for correcting for baseline shift is added to the signal generated by the magnetoresistive head to generate a baseline corrected signal. The baseline corrected signal is then monitored for positive and negative excursion from the baseline and the positive excursions are multiplied by the second correction factor and the negative excursions are multiplied by the third correction factor for generating a compensated signal.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	GB	United Kingdom	MR	Mauritania
AU	Australia	GE	Georgia	MW	Malawi
BB	Barbados	GN	Guinea	NE	Niger
BE	Belgium	GR	Greece	NL	Netherlands
BF	Burkina Faso	HU	Hungary	NO	Norway
BG	Bulgaria	IE	Ireland	NZ	New Zealand
BJ	Benin	IT	Italy	PL	Poland
BR	Brazil	JP	Japan	PT	Portugal
BY	Belarus	KE	Kenya	RO	Romania
CA	Canada	KG	Kyrgystan	RU	Russian Federation
CF	Central African Republic	KP	Democratic People's Republic of Korea	SD	Sudan
CG	Congo			SE	Sweden
CH	Switzerland	KR	Republic of Korea	SI	Slovenia
CI	Côte d'Ivoire	KZ	Kazakhstan	SK	Slovakia
CM	Cameroon	LI	Liechtenstein	SN	Senegal
CN	China	LK	Sri Lanka	TD	Chad
CS	Czechoslovakia	LU	Luxembourg	TG	Togo
CZ	Czech Republic	LV	Latvia	TJ	Tajikistan
DE	Germany	MC	Monaco	TT	Trinidad and Tobago
DK	Denmark	MD	Republic of Moldova	UA	Ukraine
ES	Spain	MG	Madagascar	US	United States of America
FI	Finland	ML	Mali	UZ	Uzbekistan
FR	France	MN	Mongolia	VN	Viet Nam
GA	Gabon				

APPARATUS FOR COMPENSATING FOR NON-LINEAR CHARACTERISTICS OF MAGNETORESISTIVE HEADS

BACKGROUND OF THE INVENTION

The present invention is generally related to magnetoresistive heads used in disk drive systems for recovering data stored on magnetic disk. In particular, the present invention relates to an apparatus for compensating for the non-linear response to flux exhibited by magnetoresistive head.

Magnetoresistive heads are read only devices that are being used in both flexible and rigid magnetic memory system, such as disk drive system, to recover data recorded on the magnetic media of the magnetic memory system. Magnetoresistive heads respond to the magnitude of the flux being sensed by the magneto-resistive head where inductive heads respond to the rate of change in flux being sensed by the inductive head. This is one of the characteristics of the magnetoresistive head that have resulted in an increase in the areal density that data can be record on the magnetic medium over that which was previously realized using inductive heads.

The magnetoresistive head has a non-linear response to the magnitude of flux as a function of the orientation of the flux. This results in the signal generated by the magnetoresistive head being asymmetrical, that is the magnitude of the positive portion of the signal will be different than the magnitude of the negative pulse portion of the signal with all other factors being constant except for the orientation of the flux. The asymmetry of the signal further cause a baseline shift in the signal due to the AC coupling employed in recovering the signal generated by the magnetoresistive head.

The combined effect of the asymmetry and baseline shift in the signal can cause a data detector, which

recovers the data from the signal, to have an increase in the number of error in the decoded data detector because typical data detector assumed a symmetrical signal with no baseline shift.

Many disk drive systems use digital data detector to recover the data from the analog signal generated by a magnetoresistive head. In such systems, an analog to digital (A/D) convertor is used to convert the analog signal into a series of digital signal which will be used by a data detector to detect the data encoded in the analog signal. The value of the digital signal is effected by the asymmetry and the baseline shift of the analog signal being sampled such that the value of the digital signal produced from the analog signal being sampled can have a different value than the digital signal would have had if the analog signal was symmetrical and had no baseline shift. The digital detectors expects the output of the analog to digital convertor to produce digital signals having specified values based upon a symmetrical analog signal with no baseline shift being provided to the analog to digital convertor. The resulting differences in value of the digital signals produced by the analog to digital convertor in response to an asymmetrical analog signal having a baseline shift can cause the data detector to erroneously interpret the digital signal produced by the analog to digital convertor.

SUMMARY OF THE INVENTION

Briefly, the present invention provides an apparatus which stores a first correction factor for correcting the baseline shift from a baseline reference, a second correction factor for correcting the peak amplitude of positive portion of the signal generated by the magnetoresistive head to a specified value and a third correction factor for negative peak amplitude of negative portion of the signal generated by the magnetoresistive head to a specified value. The

apparatus adds the first correction factor to the signal generated by the magnetoresistive head to generate a baseline corrected signal. The apparatus monitors the value of the baseline corrected signal for positive and negative excursion from the baseline reference and then multiplies the positive excursions by the second correction factor and the negative excursion by the third correction factor thereby providing a compensated signal which has been compensated for the non-linear response of the magnetoresistive head to the orientation of flux and for baseline shift.

An advantage of the invention is that the apparatus will compensate for asymmetry and baseline shift in the signal generated by a magnetoresistive head.

Another advantage of the invention is that when the compensated signal is detected by the data detector less errors will result in detected data provided by the data detector.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described with respect to the particular embodiments thereof and reference will be made to the drawings, in which:

FIGURE 1 is a block diagram of a digital apparatus for compensating for the asymmetry and baseline shift in a signal generated by a magnetoresistive head;

FIGURE 2A is a representation of an analog signal generated by a magnetoresistive head having asymmetry and baseline shift;

FIGURE 2B is a representation the analog signal of FIGURE 2A which has been corrected for base line shift; and

FIGURE 2C is a representation of the analog signal of FIGURE 2A which has been corrected for asymmetry and baseline shift.

DETAILED DESCRIPTION OF THE INVENTION

The apparatus of the invention is described in a

digital form for use between the analog to digital convertor and the digital data detector in a digital read channel. Where the disk drive system employs an analog data detector in an analog read channel or the apparatus of the invention is to be inserted prior to the digital to analog convertor in a digital read channel, it is well within the state of the art to convert the digital apparatus of the invention disclosed herein into a analog apparatus performing the same functions.

The digital apparatus of the invention is shown in Fig. 1. The analog signal generated by the magneto-resistive head is provided on line 44 to the analog to digital convertor 8. The analog signal may have been processed by the read channel but the resulting analog signal will still have the asymmetry and baseline shift of the original analog signal. The digital to analog convertor 8 receives an analog signal which is illustrated in Figure 2A. The analog signal is shown, for example purposes, as having a negative baseline shift and asymmetry where the positive excursion is greater in amplitude than the negative excursion. A positive peak signifies a point of flux reversal from a first orientation to a second orientation and a negative peak signifies a point of flux reversal from a second orientation to a first orientation. The analog signal will have a zero value when the positive and negative charges of the system coupling capacitors are balanced. Data detectors identify the positive peaks, the negative peaks and the zero values of the signal in recovering the data from the signal and expect the amplitude of the positive peak to ideally have a value of +1 and the amplitude of the negative peak to ideally have a value of -1 and the baseline to have a value of 0.

A typical disk drive system includes a plurality of magnetic disk where each side of each disks may have an associated magnetoresistive head for recovering the data recorded on that side of that magnetic disk. Therefore,

the contents of RAM 10, which is connected to microprocessor 9 by bus 30, will contain for each magnetoresistive head used in the disk drive system a first correction factor for compensating for baseline shift from a referenced baseline value, a second correction factor for correcting the amplitude of positive portion of the signal generated by the magnetoresistive head and a third correction factor for correcting the amplitude of negative portion of the signal generated by the magnetoresistive head. RAM 10 also includes a baseline reference value which is normally zero but which can be of any value designated by the designer of the disk drive system. Where the baseline reference value B is not zero then the ideal values of the positive peak will be B + A and the ideal value of the negative peak will be B - A, where A is the ideal magnitude of the positive and negative peaks.

Microprocessor 9 is connected to registers 11, 12, 13 and 14 by bus 31. When the disk drive system is first started up, microprocessor 9 will retrieve the baseline reference value from RAM 10 and will then store the value for the baseline reference value into register 13. During each head selection operation, microprocessor 9 will retrieve the first, second and third correction factors from RAM 10 for the magnetoresistive head being selected and will store the first correction factor into register 14, the second correction factor into register 11 and the third correction factor into register 12. At this time the apparatus has been initialized such that the apparatus can compensate each digital signal generated from the analog signal on line 44.

Each digital signal generated by analog to digital convertor 8 is transferred into register 15 via bus 42. Register 15 may be eliminated if the analog to digital convertor 8 maintains the value of the digital signal a sufficient length of time for the digital signal to be compensated and for an associated compensated signal to

be presented for further processing on line 43. Adder 20 adds the digital signal on bus 41 from register 15 to the first correction factor on bus 39 from register 14. Adder 20 produces a digital baseline corrected signal on bus 40.

Figure 2B shown the analog signal of FIGURE 2A after correcting the analog signal of FIGURE 2A for the baseline shift. Essentially the baseline corrected signals will have a value that would have been produced by the analog to digital convertor 8 if the analog signal of FIGURE 2B had been provided to the analog to digital convertor 8. The baseline offset must be corrected before amplitude corrections can be made.

Comparator 16 compares the baseline corrected signal on line 40 to the baseline reference value stored in register 13 on bus 36. If the baseline corrected signal is greater than the baseline reference value then comparator 16 will generate a first signal on line 38 to condition gate 18 to transfer the second correction factor on bus 32 from register 11 onto bus 33 to multiplier 19. If the baseline corrected signal is less than the baseline reference value then comparator 16 will generate a second signal on line 37 to condition gate 17 whereby the third correction factor on bus 34 from register 12 is transferred onto bus 33 to multiplier 19. If the baseline corrected signal is equal to the baseline reference value then comparator 16 will generate a first state of a third signal on line 35 to condition gate 21 to transfer the baseline corrected signal on bus 40 onto bus 43 as a compensated digital signal and to decondition gate 22. If the baseline corrected signal is not equal to the baseline reference value then comparator 16 will generate a second state of the third signal on line 35 to condition gate 22 to transfer the amplitude corrected signal on bus 44 from multiplier 19 onto bus 43 as a compensated digital signal and to decondition gate 21.

Multiplier 19 multiples the baseline corrected

digital signal on bus 40 by either the selected second or third correction factor now appearing on bus 33 to generate a amplitude corrected signal on bus 44.

Figure 2C shown the analog signal of FIGURE 2B after correcting the analog signal of FIGURE 2B for asymmetry. Essentially the amplitude corrected signal will have a value that would have been produced by the analog to digital convertor 8 if the analog signal of FIGURE 2C would had been provided to the analog to digital convertor 8.

It has been found that many magnetoresistive heads produce an asymmetrical signal where either the positive or negative peak of the asymmetrical signal has the correct amplitude and does not have to be corrected. In such a case the correction factor for the portion of the asymmetrical signal having the correct amplitude would be one and the apparatus of Figure 1 could be used as shown.

Alternatively, if all magnetoresistive heads in the disk drive system had positive peaks of the correct amplitude then no second correction factor would have to be stored in RAM 10. FIGURE 1 would be modified by deleting register 11 and gate 18. Comparator 16 would not generate the first signal to condition gate 18, the first state of the third signal would be generated when the baseline corrected signal was either equal to or greater than the baseline reference signal and the second state of the third signal would be generated when the baseline corrected signal was not either equal to or greater than the baseline reference signal.

If all magnetoresistive heads in the disk drive system had negative peaks of the correct amplitude then no third correction factor would have to be stored in RAM 10. FIGURE 1 would be modified by deleting register 12 and gate 17. Comparator 16 would not generate the second signal to condition gate 17, the first state of the third signal would be generated when the baseline corrected signal was either equal to or less than the

baseline reference signal and the second state of the third signal would be generated when the baseline corrected signal was not either equal to or less than the baseline reference signal.

Finally, if the baseline reference value was equal to zero then gates 21 and 22 may be eliminated and the compensated digital signal will always be the amplitude corrected signal from multiplier 19. Comparator 19 would condition either gate 17 or 18 when the baseline corrected signal was equal to the baseline reference value. When the baseline corrected signal is equal to zero, multiplier 19 will produce an amplitude corrected signal having the correct value of zero.

The value for the first, second and third correction factors for each magnetoresistive head in a disk drive system may be derived in many ways. Typically the correction factors are generated after the magnetoresistive heads have been installed in the disk drive system such that any effect that the electronics in the disk drive system that might have on the baseline shift or the symmetry of the analog signal might also be compensated for. Generally a program is written and run under computer control to obtain the first second and third correction factors. A data pattern is recorded on the magnetic disk, such that the time of the occurrence of the positive peaks, the negative peaks and baseline values of zero are known. The program stores the baseline reference value in register 14 and then collects a data base of a large number of digital values at the time when the baseline should have a zero value. Then a first correction factor is derived from that data base by the use of any one of a number of statistically error analysis techniques to compensate for the baseline shift in the analog signal. The first correction factor is then stored in register 14. A data base consisting of a large number of digital values for the positive peaks is collected and then a second correction factor is derived from that data base, by the use of any one of

a number of statistically error analysis techniques, for compensating the amplitude of the positive peaks to a specified value. A data base consisting of a large number of digital values for the negative peaks is collected and then a third correction factor is derived from that data base, by the use of any one of a number of statistically error analysis techniques, for compensating the amplitude of the negative peaks to the specified value.

This procedure is performed for each magnetoresistive head used in the disk drive system and the first, second and third correction factors are stored in RAM 10 at the designated address for each of the magnetoresistive heads. Of course, if the apparatus of FIGURE 1 had been modified so as not to use either the second or third correction factor, then that correction factor would not have to be generated or stored in RAM 10 for each of the magnetoresistive heads.

While the invention has been particularly shown and described with reference to the described embodiment therefore, it will be understood by those skilled in the art that changes in form and detail may be made therein without departing from the spirit and scope of the invention. Given the above disclosure of general concepts and specific embodiments, the scope of the protection sought is defined by the following.

CLAIMS

What is claimed is:

1. An apparatus for compensating for asymmetry and a baseline shift in an analog signal generated by a magnetoresistive head in a disk drive system where said asymmetry in said analog signal is in the form of positive peaks and negative peaks in said analog signal having different amplitude, said apparatus comprising:

first means for generating a baseline corrected signal from said analog signal where said baseline corrected signal is equivalent to said analog signal compensated for said baseline shift; and

second means for generating a compensated signal from said baseline corrected signal where said compensated signal has positive and negative peaks of the same amplitude and no baseline shift.

2. An apparatus for generating a digital compensated signal derived from an analog signal generated by a magnetoresistive head in a magnetic memory system where said analog signal has a baseline shift and has asymmetry in the form of positive peaks and negative peaks in said analog signal having different amplitudes, said apparatus comprising:

baseline correction means for generating a digital baseline corrected signal from said digital signal where said baseline correction signal is said digital signal corrected for said baseline shift in said analog signal; and

asymmetry correction means for generating said compensated signal from said baseline corrected signal such that said compensated digital signal will have a specified absolute value whenever said digital signal was derived from either said positive peak or said negative peak in said analog signal.

3. The apparatus of Claim 2 wherein said baseline correction means comprises;

a fourth register for storing a digital first correction factor for correcting the said baseline shift in said analog signal; and

an adder for generating said baseline corrected signal by adding said digital baseline correction signal to said digital signal whereby said baseline corrected signal has a value that said digital signal would have had if said analog signal did not have said baseline shift.

4. The apparatus of Claim 3 wherein said asymmetry correction means comprises:

a first register for storing a digital second correction factor for modifying the absolute value of said baseline corrected signal to said specified absolute value when said baseline corrected signal was derived from said digital signal which was derived from said positive peak of said analog signal;

a second register for storing a digital third correction factor for modifying the absolute value of said baseline corrected signal to said specified absolute value when said baseline corrected signal was derived from said digital signal which was derived from said negative peak of said analog signal;

a third register for storing a digital reference baseline reference value;

a selection means for providing to a multiplier said second correction factor if said baseline corrected signal was greater than said reference baseline signal or said third correction factor if said baseline corrected signal was less than said reference baseline signal; and

said multiplier for generating a digital amplitude corrected signal by multiplying said baseline corrected signal by either said second correction factor or said

third correction factor as selected by said selection means.

5. The apparatus of Claim 4 wherein said selection means comprises:

a comparator means for generating a first signal when said baseline corrected signal is greater than said baseline reference signal, a second signal when said baseline corrected signal is less than said baseline reference signal, a first state of a third signal when said baseline corrected signal is equal to said baseline reference signal and a second state of said third signal when said baseline corrected signal is not equal to said reference baseline signal;

a first multiplexor for providing to said multiplier said second correction factor in response to said first signal and said third correction factor in response to said second signal; and

a second multiplexor for providing said baseline corrected signal as said compensated signal when said comparator generates said first state of said third signal and said amplitude corrected signal as said digital compensated signal when said comparator generates said second state of said third signal.

6. The apparatus of Claim 3 wherein said asymmetry correction means comprises:

a second register for storing a digital third correction factor for modifying the absolute value of said baseline corrected signal to said specified absolute value when said baseline corrected signal was derived from said digital signal which was derived from said negative peak of said analog signal;

a third register for storing a digital reference baseline reference value;

a selection means for providing to a multiplier said third correction factor if said baseline corrected signal was less than said reference baseline signal; and

said multiplier for generating a digital amplitude corrected signal by multiplying said baseline corrected signal by said third correction factor as selected by said selection means.

7. The apparatus of Claim 6 wherein said selection means comprises:

a comparator means for generating a second signal when said baseline corrected signal is less than said baseline reference signal, a first state of a third signal when said baseline corrected signal is equal to or greater than said baseline reference signal and a second state of said third signal when said baseline corrected signal is not equal to or greater than said reference baseline signal;

a first gate for providing to said multiplier said third correction factor in response to said second signal; and

a second multiplexor for providing said baseline corrected signal as said compensated signal when said comparator generates said first state of said third signal and said amplitude corrected signal as said digital compensated signal when said comparator generates said second state of said third signal.

8. The apparatus of Claim 3 wherein said asymmetry correction means comprises:

a first register for storing a digital second correction factor for modifying the absolute value of said baseline corrected signal to said specified absolute value when said baseline corrected signal was derived from said digital signal which was derived from said positive peak of said analog signal;

a third register for storing a digital reference baseline reference value;

a selection means for providing to a multiplier

said second correction factor if said baseline corrected signal was greater than said reference baseline signal; and

said multiplier for generating a digital amplitude corrected signal by multiplying said baseline corrected signal by said second correction factor.

9. The apparatus of Claim 8 wherein said selection means comprises:

a comparator means for generating a second signal when said baseline corrected signal is less than said baseline reference signal, a first state of a third signal when said baseline corrected signal is equal to or less than said baseline reference signal and a second state of said third signal when said baseline corrected signal is not equal to or less than said reference baseline signal;

a second gate for providing to said multiplier said second correction factor in response to said first signal; and

a second multiplexor for providing said baseline corrected signal as said compensated signal when said comparator generates said first state of said third signal and said amplitude corrected signal as said digital compensated signal when said comparator generates said second state of said third signal.

10. The apparatus of Claim 3 wherein said asymmetry correction means comprises:

a first register for storing a digital second correction factor for modifying the absolute value of said baseline corrected signal to said specified absolute value when said baseline corrected signal was derived from said digital signal which was derived from said positive peak of said analog signal;

a second register for storing a digital third correction factor for modifying the absolute value of

BNSDOCID: <WO___9618189A1_I_>

said baseline corrected signal to said specified absolute value when said baseline corrected signal was derived from said digital signal which was derived from said negative peak of said analog signal;

a third register for storing a digital reference baseline value of zero;

a selection means for providing to a multiplier said second correction factor if said baseline corrected signal was greater than said reference baseline signal or said third correction factor if said baseline corrected signal was less than said reference baseline signal and either said second or said third correction factor when said baseline corrected signal was equal to said reference baseline signal; and

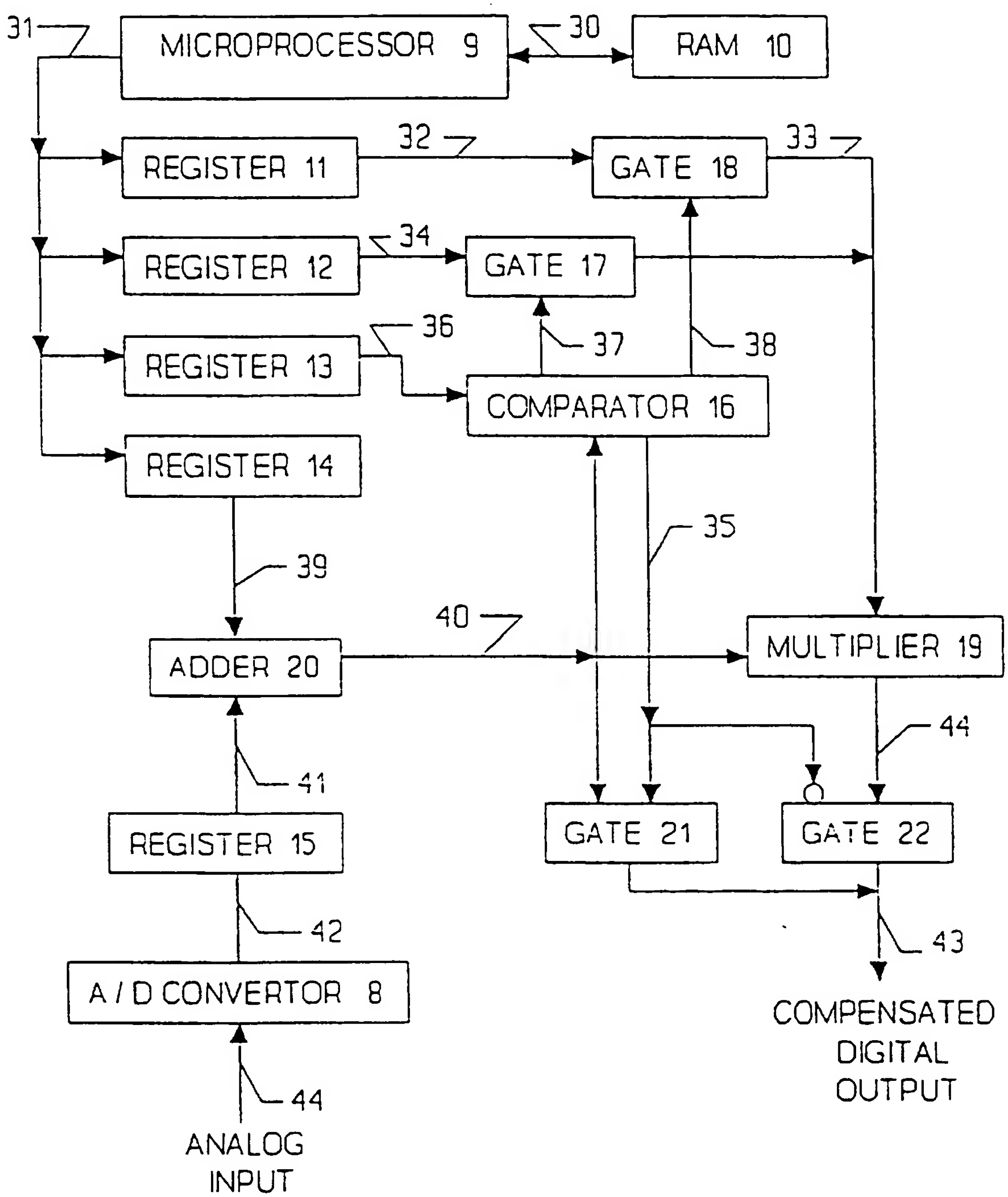
said multiplier for generating said digital compensated signal by multiplying said baseline corrected signal by either said second correction factor or said third correction factor as selected by said selection means.

11. The apparatus of Claim 10 wherein said selection means comprises:

a comparator means for generating a first signal when said baseline corrected signal is greater than said baseline reference signal, a second signal when said baseline corrected signal is less than said baseline reference signal and either said first or said second signal when said baseline corrected signal was equal to said reference baseline signal; and

a first multiplexor for providing to said multiplier said second correction factor in response to said first signal and said third correction factor in response to said second signal.

BNSDOCID: <WO___9618189A1_I_>



MICROPROCESSOR 9
RAM 10
REGISTER 11
REGISTER 12
REGISTER 13
REGISTER 14
GATE 18
GATE 17
COMPARATOR 16
MULTIPLIER 19
ADDER 20
REGISTER 15
GATE 21
GATE 22
A / D CONVERTOR 8
ANALOG INPUT
COMPENSATED DIGITAL OUTPUT
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
44

FIG. 1

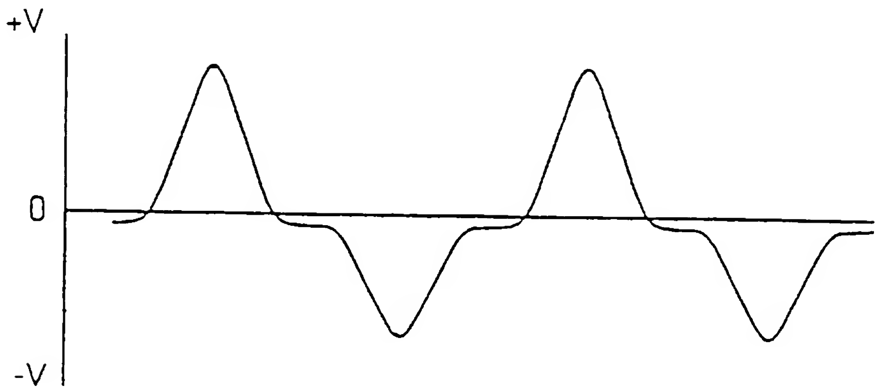


FIG. 2A

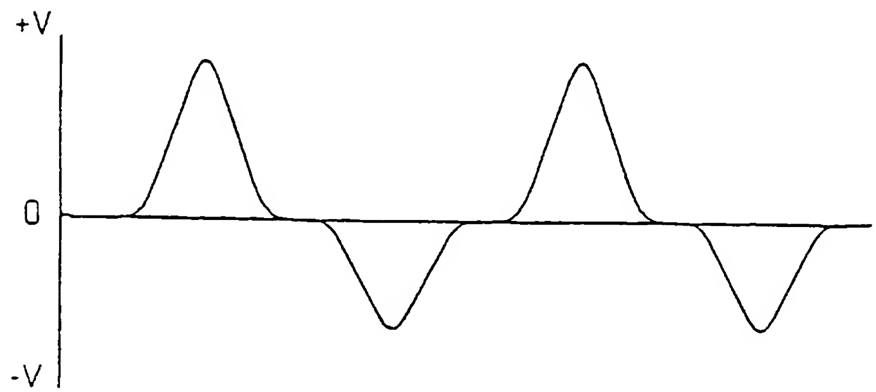


FIG. 2B

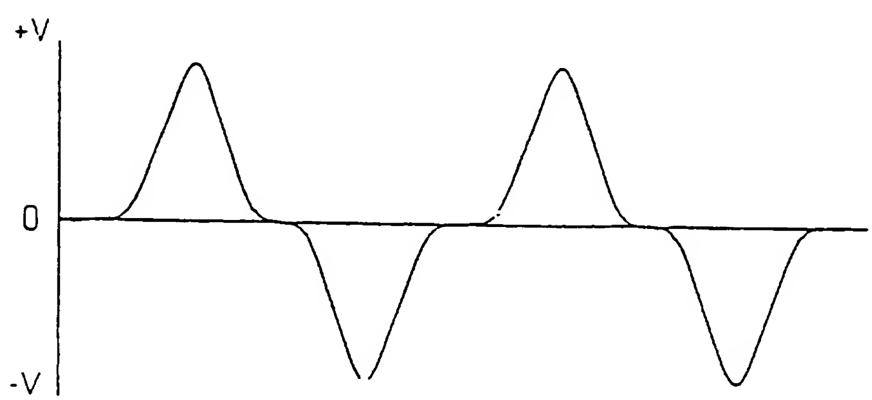


FIG. 2C

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 95/16212

A. CLASSIFICATION OF SUBJECT MATTER

G 11 B 5/39, 5/33, 5/035

According to International Patent Classification (IPC) or to both national classification and IPC 6

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G 11 B, G 01 R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US, A, 5 418 660 (SATO et al.) 23 May 1995 (23.05.95), fig. 13,21,23; abstract; claims 1-15.	1
X	US, A, 5 283 521 (OTTESEN et al.) 01 February 1994 (01.02.94), fig. 2,4,6; abstract; claims 1-13.	1
A	WO, A, 94/19 793 (IBM) 01 September 1994 (01.09.94), fig. 7; page 4, line 14 - page 5, line 7; abstract; claims 1,11,13, 16,26,27.	1-11

☐ Further documents are listed in the continuation of box C.

☐ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 March 1996	06.05.96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	BERGER e.h.

ANHANG

zum internationalen Recherchenbericht über die internationale Patentanmeldung Nr.

ANNEX

to the International Search Report to the International Patent Application No.

ANNEXE

au rapport de recherche international relatif à la demande de brevet international n°

PCT/US 95/16212 SAE 123897

In diesem Anhang sind die Mitglieder der Patentfamilien der im obengenannten internationalen Recherchenbericht angeführten Patentdokumente angegeben. Diese Angaben dienen nur zur Unterrichtung und erfolgen ohne Gewähr.

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The Office is in no way liable for these particulars which are given merely for the purpose of information.

La presénte annexe indique les membres de la famille de brevets relatifs aux documents de brevets cités dans le rapport de recherche international visée ci-dessus. Les reseignements fournis sont donnés à titre indicatif et n'engagent pas la responsibilité de l'Office.

Im Recherchenbericht angeführtes Patentdokument Patent document cited in search report Document de brevet cité dans le rapport de recherche	Datum der Veröffentlichung Publication date Date de publication	Mitglied(er) der Patentfamilie Patent family member(s) Membre(s) de la famille de brevets	Datum der Veröffentlichung Publication date Date de publication
US A 5418660	23-05-95	JP A2 5205205	13-08-93
		JP A2 5159209	25-06-93
US A 5283521	01-02-94	CN A 1083957	16-03-94
		CN B 1028685	31-05-95
		GB A0 9308307	09-06-93
		GB A1 2267383	01-12-93
		GB B2 2267383	07-02-96
		JP A2 6044510	18-02-94
WO A1 9419793	01-09-94	BR A 9400133	04-10-94
		CA AA 2102087	19-08-94
		CN A 1096607	21-12-94
		EP A1 685103	06-12-95
		HU A0 9502416	30-10-95
		JP A2 6259739	16-09-94
		PL A1 310176	27-11-95
		US A 5455730	03-10-95

BNSDOCID: <WO___9618189A1_I_>